LIBRARY ieee ;

USE ieee.std\_logic\_1164.all ;

ENTITY lab6d IS

PORT ( w0, w1, w2, w3 : in std\_logic;

s : IN STD\_LOGIC\_vector (1 downto 0) ;

f : OUT STD\_LOGIC ) ;

END lab6d ;

ARCHITECTURE Behavior OF lab6d IS

BEGIN

PROCESS ( w0, w1,w2, w3, s)

BEGIN

CASE s IS

WHEN "00" => f <= w0 ;

WHEN "01" => f <= w1;

WHEN "10" => f <= w2;

WHEN OTHERS =>

f <= w3 ;

END CASE ;

END PROCESS ;

END Behavior ;